PLL frequency synthesizers 101

Part 1 of 2, explaining the basics of how a PLL frequency synthesizer works.

Part one contains the principles of how the different parts of it operate, and finishes with a real world example - the Uniden uPD858.

Part two contains the variations for different chassis and additions used in modern circuitry.

Note: Some details have been simplified to illustrate a principle. These simplifications will be covered in part 2.

Preface

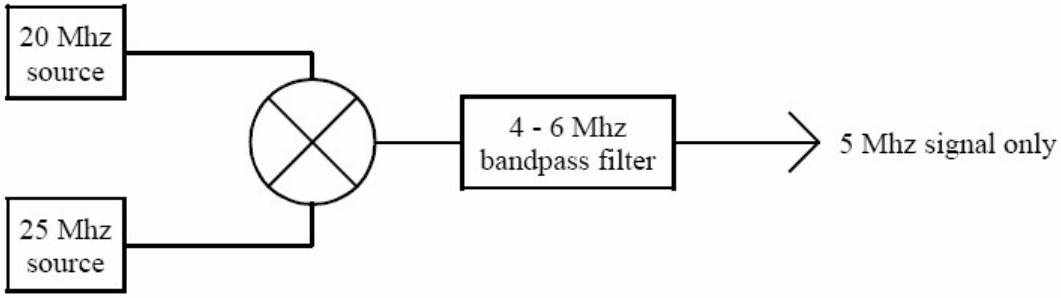
The process of frequency changing is fundamental to understanding how a PLL works, and must be understood to successfully perform faultfinding. Frequency changing by mixing and multiplication are used multiple times in a typical radio, so before the PLL you will need to know the basics of mixers, multipliers, and superhetrodyne radio operation.

This has been scanned from an old uni 101 paper and edited to include the 858.
PM me if you find any OCR errors…

Mixers

Whenever two frequencies are combined into a non-linear device, two **new** frequencies are produced.
The two new frequencies are the **sum** (the two added together) and the **difference** (the lowest one subtracted from the highest).

For example: Mixing a 20 Mhz and a 25 Mhz signal results in 4 frequencies:
- The original 20 Mhz signal
- The original 25 Mhz signal
- a new 45 Mhz signal (20 + 25)
- a new 5 Mhz signal (25 – 20).

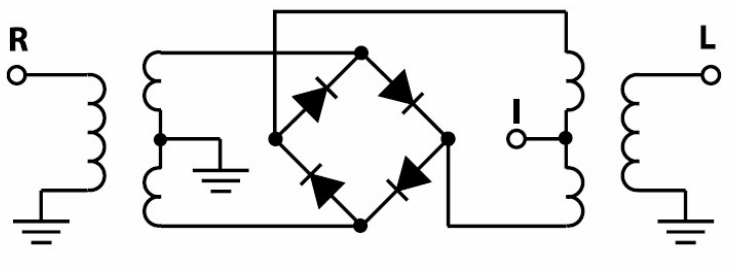


Only one of the 4 will be the desired frequency. A filter always follows a mixer, this will allow the wanted signal to pass through and the other unwanted signals to be rejected. In the above example, only the 5 Mhz signal was wanted, and the passband of the filter was chosen to accomplish this.

Balanced and double-balanced mixers

A limitation of the simple example above is the lack of isolation between the 2 inputs and the outputs.

A double balanced mixer, using four diodes and a pair of balun transformers, can be used to overcome this.



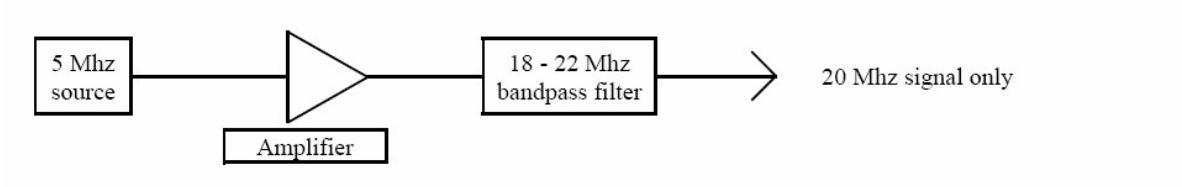
Some local oscillator energy appears at the input of the transformer, but is anti-phase and cancels.
For example, a voltage on terminal "L" is induced into the windings either side of terminal "I", but they are of opposite polarity and cancel out.

Double balanced mixers require precision windings and a well matched set of 4 diodes, which makes this method expensive. Because of the added cost, they are rarely seen on CB equipment, but are common on military, commercial, and better quality ham gear.

Multipliers

Normally, when an amplifier circuit is designed, it is made to be as clean as possible. The output waveform looks larger but is the same shape as the input. If a waveform is deliberately over driven to a distorted state, harmonics will be produced. These are multiples of the input frequency. If a relatively narrow filter placed at the output, a frequency that is a known multiple of the input can be created.

Why would anyone want to do this? One reason is that it's easier (cheaper) to make stable crystals up to about 16 Mhz, and sometimes we need higher frequencies from a crystal. In the case of the Uniden SSB chassis, we need 33 Mhz (more on this later) - higher than our 16Mhz limit. Uniden overcame this by using 11Mhz crystals and tripling their output to 33 Mhz.



In the above example, a 5 Mhz signal is over-driven. Outputs will be present at 5 Mhz, 10 Mhz, 15 Mhz, 20 Mhz, 25 Mhz, and so on. If a filter that only passes 18 to 22 Mhz is placed on the output, only the 20 Mhz signal passes through. We now have an output that is quadruple the input frequency.

If the input signal is changed to 4.75 Mhz, the output will drop to 19 Mhz, which is still exactly quadruple the input frequency. The input frequency can only be changed to the point where the multiplied output will be within the bandpass of the output filter, therefore multipliers can only operate over a relatively narrow band of frequencies.

In some cases the filter directly after the multiplier can be eliminated - for example when the output of the multiplier is sent to one input of a mixer, which is in turn followed by a filter.

Dividers

These will be shown here as a simple "box" with two inputs (one analog and one digital) and one analog output. You don't need to know how how this section works, just what it does, in order to understand the PLL.

The analog input is a frequency, the digital input is the number that the input will be divided by - for example, a 5Mhz input with a "number" input of 125 will give an output of 40 Khz. This is because 5Mhz is just another way of saying 5000Khz, and 5000 divided into 125 is equal to 40.

Frequency dividers and multipliers cannot be used where amplitude-modulated information needs to be retained.

Note: from now all frequencies will be shown in Khz to keep the math simple (no Mhz to Khz and back to Mhz conversions needed), so channel 19 will be shown as "27185 Khz".

Superhetrodyne receivers and transmitters - the basics

Human speech operates over a range of 0.3 to 3 Khz, called the **baseband**. Humans can communicate directly with this range using their vocal cords and their ears.

The problem with baseband is that it doesn't travel far, a hundred yards under ideal conditions is about the best you can hope for. To send your voice over a longer distance without wires, it needs to be changed to a radio frequency (**RF**) signal. At CB, this is around the 27000Khz area.

Some RF signal processing - such as very high gain amplification and generation of SSB signals - works best at a very narrow range of frequencies, known as the "intermediate frequency".

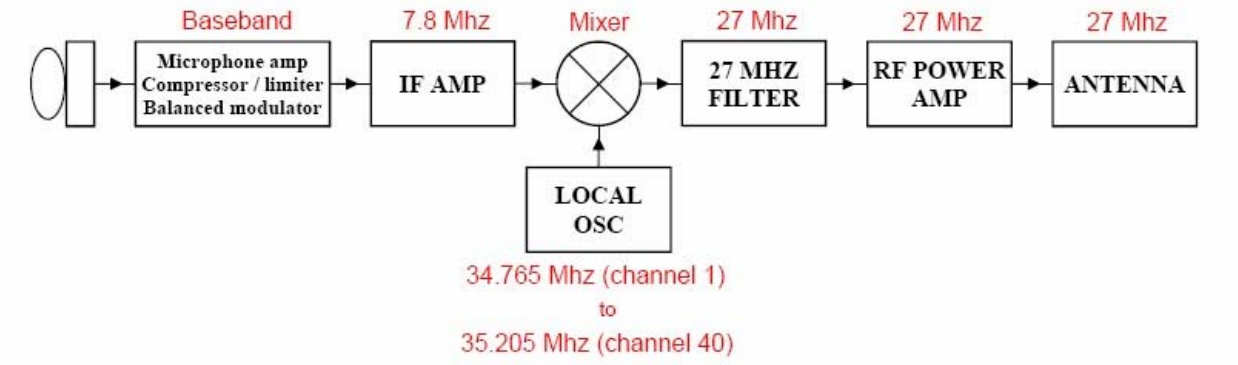
This narrow range is abbreviated to **IF** - for example, an "IF transformer" is a transformer designed to operate over a very narrow range of frequencies.

Some signals carry NO information at all, they are just unmodulated carriers. These are fed into one input of a mixer for the purposes of frequency changing. These carrier signals are known as the "local oscillator", or **LO.**

A theoretical radio will be used to explain this - an AM only version of the 858 SSB chassis.

Deliberate simplifications: The slight frequency offsets for LSB/USB are not shown, and it uses low level modulators for all modes.

Transmit



Microphone audio is filtered, compressed, and limited to optimize it for speech and keep the radio within legal limits set by the FCC. This is done at baseband, which is the same frequency as what comes out of our mouths when we talk.

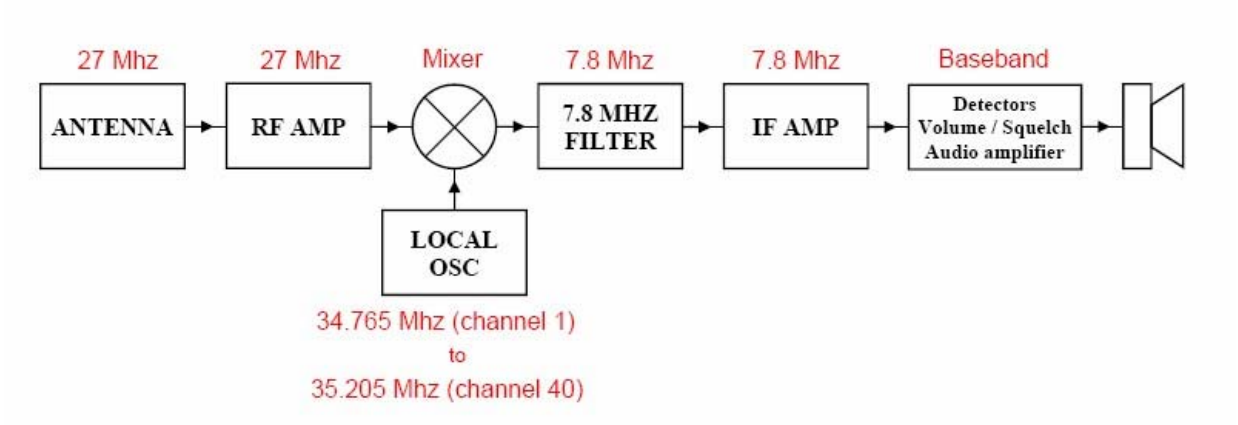
The balanced modulator them modulates the voice signal onto a carrier at 7800 Khz.

We now have a low level signal centered about 7.8 Mhz, modulated with our voice. This signal in then amplified (buffered) and sent to the mixer.

An unmodulated LO signal is sent to the other input of the mixer, where it mixes with the voice modulated at 7.8Mhz. The difference frequency (LO - IF) is filtered out - for example, if the LO is at 34.765, the difference output is exactly 7.8Mhz lower.

34.765 - 7.8 = 26.965, which is CB channel 1. This is then fed to a power amplifier and then to the antenna for transmission.

Receive



The antenna receives signals on all channels. This mixture of signals is passed through an RF amplifier and then to one input of a mixer.

For the purposes of this explanation, the antenna is picking up two transmissions, one on channel 1 (26.965) and the other on channel 19 (27.185).

Both of these signals are amplified and enter the mixer.

An unmodulated LO signal (34.765 Mhz if the radio is set to channel 1) is sent to the other input of the mixer, where it mixes with the two incoming signals. Both appear at the output of the mixer, at 7.8 Mhz (34.765 - 26.965) and 7.58 Mhz (34.765 - 27.185).

A filter, straight after the mixer, lets the 7.8 Mhz signal pass through and blocks the unwanted 7.58 Mhz one from the station operating on channel 19.

Only the signal from channel 1 - the channel that the radio is set to - has been passed.

This 7.8 Mhz signal is then converted back to baseband and amplified / sent to the speaker. It is also measured for strength. The results of this measurement are used to operate the squelch function, and to drive the radios signal meter.

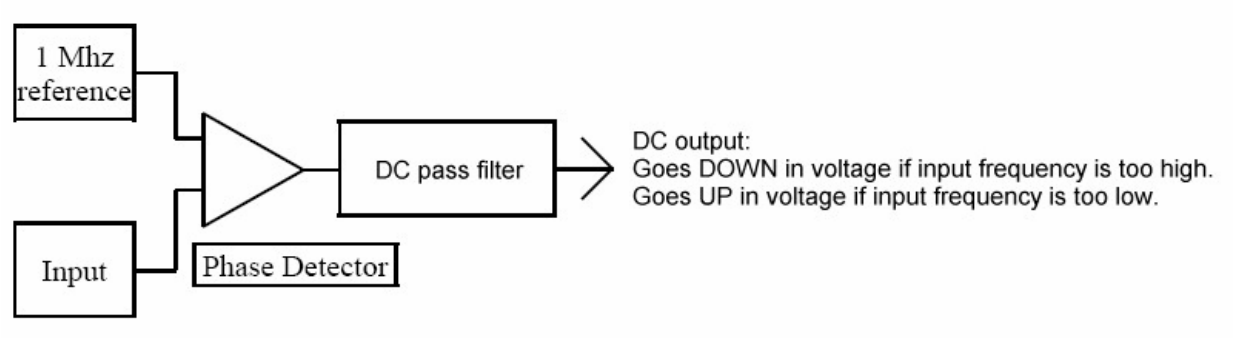
In both the transmit and receive sections, we only need to make one change - the LO signal - to change the operating frequency of the radio. In this simple example, the LO frequency is the same for transmit and receive. In many designs, there is a shift - this will be covered in part 2.

You should now be comfortable with **RF**, **IF**, **LO**, and **baseband**. If not, re-read the notes or ask.

All we need to know now is how to generate the LO signal. This is the job of the PLL synthesizer.

The PLL

The heart of the PLL circuitry is a section called a "Phase detector". This does for an AC signal what a comparator does for DC. It has two inputs, and it compares the two incoming frequencies.



The first (top in this example) is a constant input and never changes - in this case, it's a constant 1Mhz signal from a crystal oscillator.

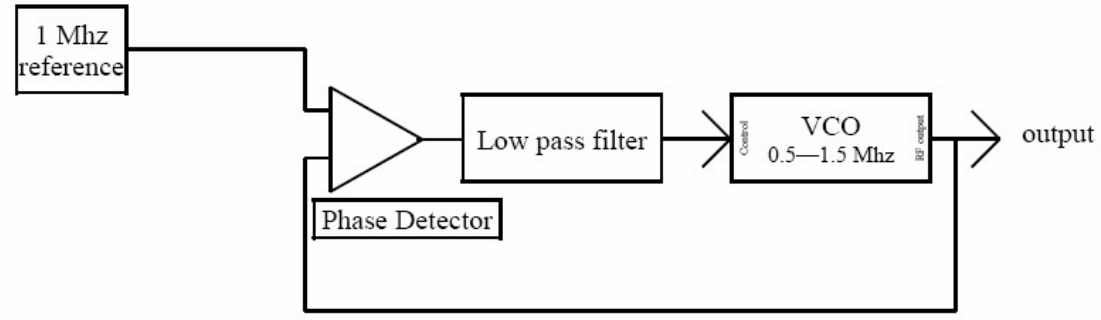
The second input is variable.
If it is LOWER than the first, the output pulses high (towards the supply voltage, usually 5V).
If it is HIGHER than the first, the output pulses low (towards zero volts).

The output is a series of pulses which need to be heavily filtered back to a nice smooth DC signal.
This DC voltage can vary anywhere from 0 to 5V.

The VCO

This is just an oscillator that can have its frequency changed be varying a DC "control voltage".

The one below can be varied from 0.5 Mhz to 1.5 Mhz continuously by setting it's control voltage.
At around the middle of it's control voltage range (2.5V) it will be at the middle of its frequency range (1 Mhz).



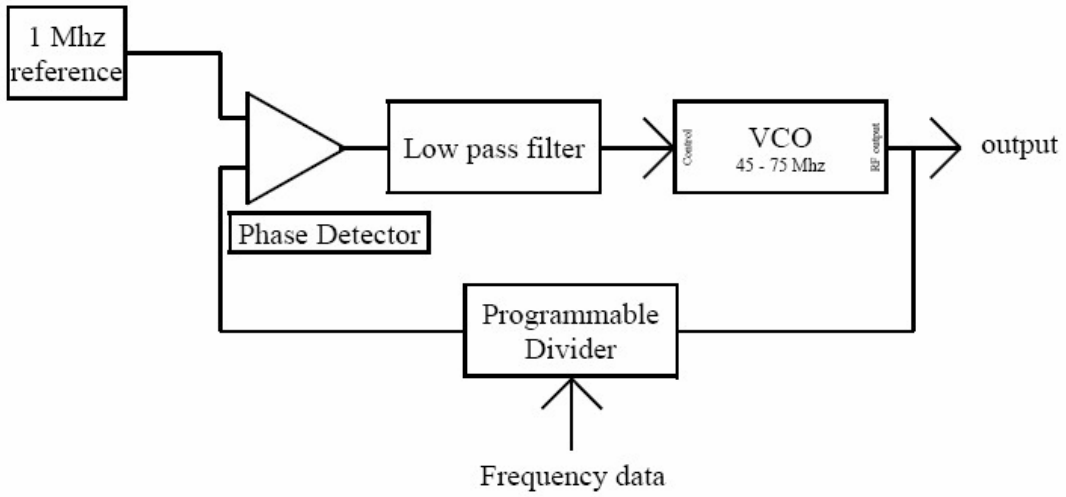
Two circuit sections from the previous sections have now been combined into one unit.
Note that a sample of the VCOs output is fed back into the phase detector as the “second frequency”.

When the circuit is first powered up, the tuning voltage will be at zero volts, and the phase detector output will go high (because the reference frequency is the higher of the two inputs).

The VCO frequency will gradually (within a few milliseconds) rise until the output goes over 1 Mhz, at which point the output of the phase detector will go low. The VCO will start to reduce in frequency, again until it crosses the 1 Mhz point. These cycles will continue a few more times (a millisecond or two) until the VCO eventually settles on a frequency of exactly 1 Mhz.

The low pass filter slows down the process slightly to prevent the VCO going into an endless cycle of over-corrections. The loop is then said to be “locked” - this simply means that the two inputs to the phase detector are in phase and on the same frequency. If the VCO drifts off frequency, the change will be sensed by the phase detector, and the tuning voltage will be changed to bring it back onto the same frequency as the reference.

At this point, however, we have only managed to “copy” a frequency, not create a new one.



A “Programmable divider” is now added to the circuit. The VCO has also been changed, to one that can change from 45 to 75 Mhz for its 0V to 5V control range - at 2.5V, it would be at its halfway point of 60 Mhz.

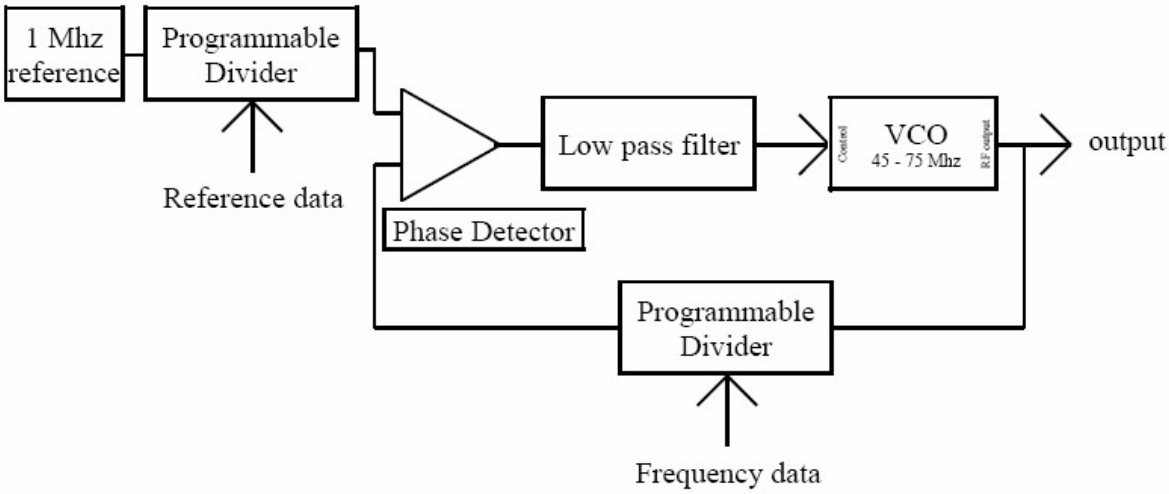
In this example, the programmable divider can be set to any division ratio from 1 to 99. If set for a ratio of 50, the VCO will settle at 50 Mhz (1 Mhz x 50) as this frequency will satisfy the condition of the same frequency appearing at both inputs of the phase detector. By changing the divider for a value of our choice from 45 to 75, any frequency from 45 to 75 Mhz, in 1 Mhz steps, can be created.

If we try and push it too far, a fault condition will be created. If the programmable divider is set to 80, the phase detector will go to maximum output and drive the VCO to its top limit of 75 Mhz.

The loop is now "out of lock" and the PLL circuit is no longer controlling the VCO frequency.

Most PLL ICs can detect this condition and will disable the transmitter (and sometimes the receiver) if an out-of-lock fault occurs.

The 1 Mhz step size is too large for most uses, however a second divider can be added between the 1 Mhz reference and the phase detector to overcome this.



The second divider has now been added. The two are loaded with data that would give the desired frequency of operation, for example:

Reference divider = 1000 Programmable divider = 50,000:
Ref / 1000 = 1 Khz VCO /50,000 = 1 Khz
As 50,000 x 1 Khz is 50 Mhz, the loop will settle at 50 Mhz as it did in the previous example.
However, we can now program the VCO to operate in much smaller “steps” of frequency than we could in the previous circuit.

If we change the programmable divider to 50,010, the VCO will shift to 50.010 Mhz, because the output of the phase detector will rise until it sees exactly 1Khz at the bottom input. This will occur when the VCO (50.010 Mhz) is divided by 50,010.

Divider speed

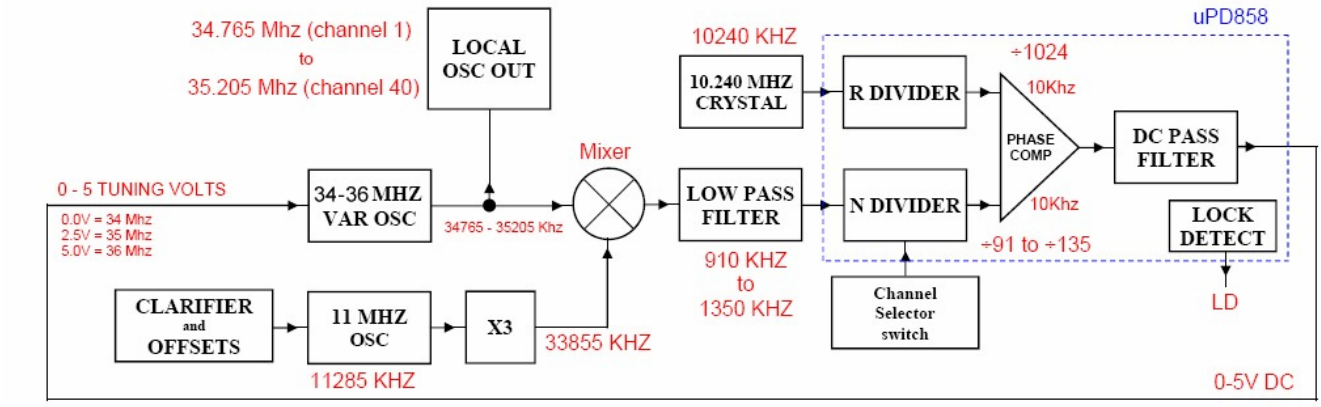
Earlier dividers, such as those used on the PLL02A, uPD858, and the MB8719 were CMOS types limited to about 5 Mhz. This was too low to divide the LO signal directly, so a second mixer was used to down-convert the LO to something that the divider could handle.

In the earlier Uniden "858" chassis, a local oscillator in the 34765 to 35205 was used.

An 11285 crystal was tripled to 33855 and mixed with the LO.

This gave an output of 910 to 1350 Khz to the divider, well within the 5Mhz (5000Khz) limitation of the IC.

Putting it all together



The diagram shows the frequencies present in AM receive mode on the 858 SSB chassis.
Not shown are the other two 11Mhz crystals used for SSB and AM transmit (this will be shown in part 2).

When the radio is first turned on, with the channel selector set to channel 1, there is no voltage (0.0V) on the control line at the bottom of the drawing. This sets the LO to its minimum value of 34 Mhz.

This mixes with the 33.855, giving 0.145 Mhz at the input to the N divider.

This is then divided by 91, giving 1.6 Khz at the bottom input of the phase comparator.

The other (fixed) input to the phase comparator is at 10 Khz, causing a mismatch. Because the variable input is too low, the output voltage rises. The control voltage increases until the bottom input is at 10 Khz (the same frequency as the top input).

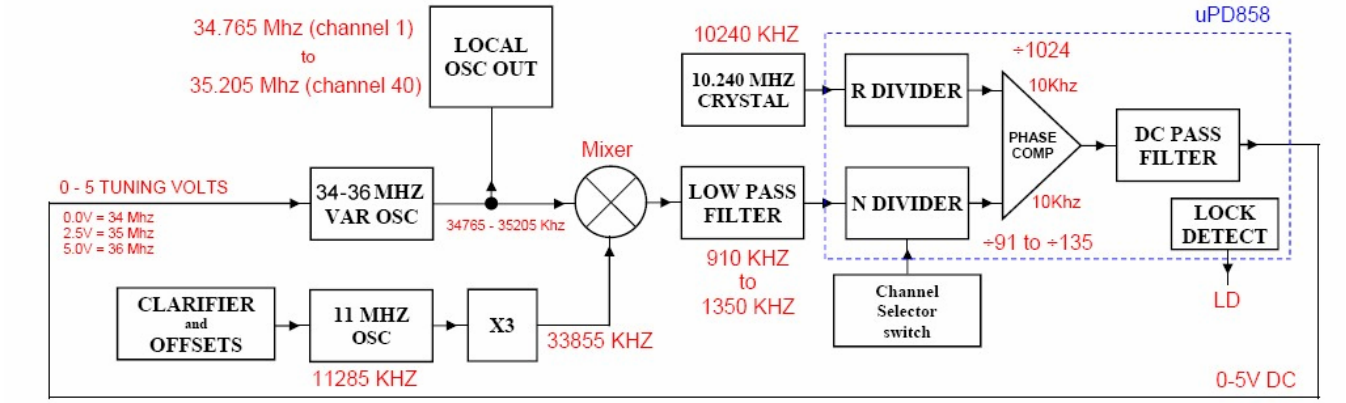
This happens when the LO reaches 34.765 Mhz, because 34.765 - 33855 = 910 Khz,
and 910 Khz divided by 91 = 10 Khz.

If it goes too far (the LO frequency goes higher than 34.765), then the bottom input will rise to above 10Khz. This causes the DC control voltage to fall, bringing the LO back to the correct frequency.

The whole process from turn on to "locked" takes just a fraction of a second.

With the LO output now at a steady 34.765 Mhz, the radio is ready for use.

On receive, 34.765 mixes with our incoming signal at 26.965, sending the correct 7.8 Mhz IF signal to the detector. On transmit, it mixes with the 7.8 Mhz carrier oscillator, causing the radio to transmit on 26.965 Mhz.



The owner of the radio now decides he wants to listen to channel 19, so he / she turns the knob until "19" shows on the display. The channel selector also sends a value of 113 to the N divider when they do this.

The LO is still at 34.765 Mhz, this is mixed down by 33.855 to 0.91 Mhz (910 Khz) and divided by 113, giving 8 Khz at the bottom input of the phase comparator. Because the variable input is too low, the output voltage rises. Again, the control voltage increases until the bottom input is at 10 Khz.

This happens when the LO reaches 34.985 Mhz, because 34.985 - 33855 = 1130 Khz, and 1130 Khz divided by 113 = 10 Khz. Again, this happens in the blink of an eye.

With the LO output now at a steady 34.985 Mhz, the radio is ready for use.

On receive, 34.985 mixes with our incoming signal at 27.185, sending the correct 7.8 Mhz IF signal to the detector. When the user transmits a reply, the LO mixes with the 7.8 Mhz carrier oscillator, giving 27.185 Mhz, in other words channel 19.

Reduction of pin count

The cost of a switch and IC for the PLL selector goes up whenever more wires are added. Less wires = less cost, significant savings can be had when you make millions of radios.

Governments also wanted to stop people adding illegal frequencies. Solve both by adding a digital number converter called a "ROM block" inside the IC.

You need at least 6 wires for 40 channels (5 wires allow 32 combinations, 6 wires give a maximum of 64), so by restricting manufactures to 6 wires, it restricted radios to a maximum of 64 channels (the MB8734 is an example of this).

By adding only legal frequency combinations to the ROM block, this was reduced to exactly 40 channels.

Serial data transfers send all of the frequency information along one wire, this could be dozens of bits (i.e. millions of combinations), but you will need to be an expert on digital electronics to modify one of these.

The MC145170 can be used to replace most "restricted" PLL chips, giving more than 64000 "channels", far more than the radio will ever handle, but you'll need to manipulate serial data to do this mod.

By using a modern serial PLL and a cheap microcontroller to replace an older or ROM locked PLL, many more frequencies (such as 10 meter ham) can be added. The limiting factor for the number of channels is now the radios RF stages and the tuning range of the oscillator used to generate the LO signal.

A stock radio will cover 0.8 to 1.6 Mhz, but additional mods can increase this about 3 to 4 Mhz before it becomes impractical.

Coming soon to part 2: variations on the basics...